Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **OUTPUT**
2. **V+**
3. **IN-**
4. **IN+**
5. **V-**

**.028”**

**4**

**2 1 5**

**5**

**MASK**

**REF**

**L**

**M**

**H**

**6**

**6**

**0**

**9**

**B**

**.041”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size = .004 x .004”**

**Backside Potential: V- or FLOAT**

**Mask Ref: LMH6609B**

**APPROVED BY: DK DIE SIZE .028” X .041” DATE: 7/7/22**

**MFG: NATIONAL THICKNESS .016” P/N: LMH6609B**

**DG 10.1.2**

#### Rev B, 7/1